531 Rec'd PCT/PTO 07 DEC 2001

FORM PTO-1390 OFFICE (REV. 11-2000) — U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK	ATTORNEY'S DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371	32860-000204/US
	U.S. APPLICATION NO. (If known, see 37 CFR 1.5) NEW 10/090893

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/01712	May 26, 2000	June 8, 1999

TITLE OF INVENTION
INTERFACE FOR COUPLING A BUS NODE TO THE BUS LINE OF A BUS SYSTEM

APPLICANT(S) FOR DO/EO/US
Norbert FICHTNER and Dieter MUNZ

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39 (1).
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau). WO 00/75794 A1
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is transmitted herewith.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4)
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 20. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98-1449 and International Search Report (PCT/ISA/210) in German with five (5) references.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☒ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information:
    1) One (1) sheet of Formal Drawings
    2.) Article 34 Amended Specification and Claims

10030893 . 040902

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U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
NEW 10/030893	PCT/DE00/01712	32860-000204/US

21. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO. **$1,040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO. **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4). **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ **890.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ **130.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	18 - 20 =	0	X **$18.00**	$ **0**	
Independent Claims	1 - 3 =	0	X **$80.00**	$ **0**	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)		None	+ **$270.00**	$ **0**	
			TOTAL OF ABOVE CALCULATIONS =	$ **1,020.00**	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$ **0**	
			SUBTOTAL =	$ **1,020.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$ **0**	
			TOTAL NATIONAL FEE =	$	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
			TOTAL FEES ENCLOSED =	$ **1,020.00**	
			Amount to be: refunded	$	
			charged	$	

a. ☐ A check in the amount of $ _____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account. No. 08-0750 in the amount of $1,020.00 to cover the above fees. A triplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 08-0750.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

Send all correspondence to:
Harness, Dickey & Pierce, P.L.C – Customer No. 30596
Post Office Box 8910
Reston, Virginia 20195

Date: December 7, 2001

By _____
Donald J. Daley, #34,313

/kna

BOX PCT
PATENT
32860-000204/US

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicants:	Norbert FICHTNER and Dieter MUNZ
Int'l Application No.	PCT/DE00/01712
Application No.:	**NEW**
Filed:	December 7, 2001
For:	INTERFACE FOR COUPLING A BUS NODE TO THE BUS LINE OF A BUS SYSTEM

PRELIMINARY AMENDMENT

BOX PCT
Assistant Commissioner for Patents
Washington, DC 20231

December 7, 2001

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application.

IN THE ABSTRACT OF THE DISCLOSURE

Please replace the original Abstract with the attached revised Abstract.

IN THE SPECIFICATION

Please replace the Specification with the attached Substitute Specification attached hereto.

IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) An interface for coupling a bus node to a bus line of a bus system comprising:

an input for an external supply voltage, supplied by a voltage source which is independent of the bus; and

a monitoring circuit for comparing an internal supply voltage, derived from the bus voltage using the external supply voltage, and for generating an output control signal for the bus node based upon a result of the comparison.

2. (Amended) The interface as claimed in claim 1, wherein the output control signal is a binary signal whose value is determined by a sign of a difference between an internal reference voltage and an external reference voltage, respectively derived from the internal supply voltage and the external supply voltage.

3. (Amended) A bus system comprising an interface as claimed in claim 1, and including a voltage source, independent of the bus line, for supplying at least one bus node.

4. (Amended) The bus system comprising an interface as claimed in claim 1, wherein, in the case of a bus subscriber which is supplied by the internal supply voltage, the input for the external supply voltage is short-circuited to the voltage output of the internal supply voltage.

Please add the following new claims:

-- 5. A bus system comprising an interface as claimed in claim 2, and including a voltage source, independent of the bus line, for supplying at least one bus node.

6. The bus system comprising an interface as claimed in claim 2, wherein, in the case of a bus subscriber which is supplied by the internal supply voltage, the input for the external supply voltage is short-circuited to the voltage output of the internal supply voltage.

7. An interface for coupling a bus node to a bus line of a bus system comprising:

an input means for receiving an external supply voltage, supplied by a voltage source which is independent of the bus; and

a monitoring means for comparing an internal supply voltage, derived from the bus voltage using the external supply voltage, and for generating an output control signal for the bus node based upon a result of the comparison.

8. The interface as claimed in claim 7, wherein the output control signal is a binary signal whose value is determined by a sign of a difference between an internal reference voltage and an external reference voltage, respectively derived from the internal supply voltage and the external supply voltage.

9. A bus system comprising an interface as claimed in claim 7, and including a voltage source means, independent of the bus line, for supplying at least one bus node.

10. A bus system comprising an interface as claimed in claim 8, and including a voltage source means, independent of the bus line, for supplying at least one bus node.

11. The bus system comprising an interface as claimed in claim 7, wherein, in the case of a bus subscriber which is supplied by the internal supply voltage, the input means for the external supply voltage is short-circuited to the voltage output of the internal supply voltage.

12. The bus system comprising an interface as claimed in claim 8, wherein, in the case of a bus subscriber which is supplied by the internal supply voltage, the input means for the external supply voltage is short-circuited to the voltage output of the internal supply voltage. --

REMARKS

Claims 1-12 are now present in this application, with new claims 5-12 being added by the present Preliminary Amendment. It should be noted that the amendments to original claims 1-4 of the present application are non-narrowing amendments, made solely to place the claims in proper form for U.S. practice and not to overcome any prior art or for any other statutory considerations. For example, amendments have been made to broaden the claims; remove reference numerals in the claims; remove multiple dependencies in the claims; and to place claims in a more recognizable U.S. form, including the use of the transitional phrase "comprising" as well as the phrase "wherein". Other such non-narrowing amendments include reorganizing apparatus-type claims (setting forth elements in separate paragraphs) in a more recognizable U.S. form. Again, all amendments are non-narrowing and have been made solely to place the claims in proper form for U.S. practice and not to overcome any prior art or for any other statutory considerations.

SUBSTITUTE SPECIFICATION

In accordance with 37 C.F.R. §1.125, a substitute specification has been included in lieu of substitute paragraphs in connection with the present Preliminary Amendment. The substitute specification is submitted in clean form, attached hereto, and is accompanied by a

marked-up version showing the changes made to the original specification. The changes have been made in an effort to place the specification in better form for U.S. practice. No new matter has been added by these changes to the specification. Further, the substitute specification includes paragraph numbers to facilitate amendment practice as requested by the U.S. Patent and Trademark Office.

CONCLUSION

Accordingly, in view of the above amendments and remarks, an early indication of the allowability of each of claims 1-12 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, P.L.C

By: _____
Donald J. Daley, Reg. No. 34,313

P.O. Box 8910
Reston, Virginia 20195
(703) 390-3030

DJD:kna

ABSTRACT OF THE DISCLOSURE

An interface for coupling a bus node to the bus line of a bus system includes an input for an external supply voltage which is made available by a voltage source, independent of the bus. A monitoring circuit is included for comparing an internal supply voltage which is derived from the bus voltage with the external supply voltage, and for generating an output control signal for the bus node as a function of the result of the comparison.

Description

PCT

Interface for coupling a bus ~~user~~ node to the bus line of a bus system

FIELD OF THE INVENTION

The invention generally relates to an interface for coupling a bus ~~user~~ node to the bus line of a bus system, ~~in particular~~ More specifically, it relates to an interface Preferably, it relates to the bus system EIB of the European Installation Bus Association EIBA.

BACKGROUND OF THE INVENTION

The bus system EIB is a two-wire bus system in which the voltage supply of the bus ~~users~~ nodes, which are respectively connected to the bus system via an interface, and the data transmission between the latter are combined on one pair of lines. In this type of bus system, the power drain per bus ~~user~~ node is limited to 10 mA, for example. However, such a limited power drain is not sufficient for all the bus ~~users~~ nodes in all applications, ~~so that~~ Thus, it may be necessary to supply an external voltage to bus users with a higher power requirement. Such an additional external supply voltage which is independent of the bus can also be advantageous for relieving the loading on the voltage supply of the EIB.

In such a case, the situation arises in which, although the interface, for example a TPUART-IC, is supplied from the EIB cell, the bus ~~user~~ node which is connected to the bus system via this interface is fed from an external voltage supply which is independent of the latter.

An interface which is used with the EIB generates a control signal (reset signal) for the bus ~~user~~ node with which, inter alia, the exchange of data is enabled only if the supply voltage of the bus ~~user~~ node has reached a predefined value, and the bus ~~user~~ node has also been given sufficient time for a correct run-up. When

there is no bus voltage, or insufficient bus voltage, the interface outputs a value

for a binary control signal, for example low (= reset active), which ensures that an exchange of data cannot take place. The control signal is not set to another value, for example high (= reset inactive) and an exchange of data made possible until both the supply voltage of the interface and the bus voltage which is transmitted from the interface to the bus ~~user~~ node has reached a predefined value.

In the case of a bus ~~user~~ node which is supplied via an external power supply unit, an operating situation may then occur in which, on the one hand, the bus voltage is not yet present at a sufficient level, ~~but,~~ on the other hand, the external voltage supply for the bus ~~user~~ not is already present so that the bus ~~user~~ node is active, but the interface itself has not yet been supplied with a sufficient supply voltage necessary for its operation. In this case, an attempt by the bus ~~user~~ node to transmit would lead to a fault message.

JP 01 193 953 A discloses a system for detecting abnormality of bus, and DE 196 39 635 C discloses a CMOS bus driver circuit.

SUMMARY OF THE INVENTION

The invention is ~~then~~ based on ~~the~~ an object of disclosing an interface for coupling a bus user to the bus line of a bus system, preferably one with which the faulty operating state specified above is avoided.

The ~~aforesaid~~ object is achieved, for example, by ~~according to~~ the invention with an interface having the features of patent claim 1. The interface preferably ~~according to the invention~~ contains an input for an external supply voltage which is made available by a voltage source which is independent of the bus, and a monitoring circuit for comparing an internal supply voltage which

is derived from the bus voltage with the external supply voltage, and for generating an output control signal for the bus ~~user~~ node as a function of the result of the comparison. This measure ensures that the bus ~~user~~ node is enabled only if the interface is also in a satisfactory operating state.

In one preferred embodiment of the invention, the output control signal is a binary signal whose value is determined by the sign of the difference between an internal reference voltage and an external reference voltage, respectively derived from the internal supply voltage and the external supply voltage. Such an interface ~~according to the invention~~ is preferably provided in particular for use in a bus system which contains at least one bus ~~user~~ node which is supplied with an external supply voltage from a voltage source which is independent of the bus.

The interface ~~according to the invention~~ preferably cannot be used for coupling a bus user supplied by the bus voltage. For this purpose, in one advantageous configuration of the invention, all that is necessary is to short-circuit the input of the external supply voltage to an output for the internal supply voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to explain the invention further, reference is made to the exemplary embodiment in the drawing, in which:

FIG 1 shows an interface according to the invention with a bus ~~user~~ node connected thereto, in a block circuit diagram,

FIG 2 shows an advantageous configuration of a monitoring circuit for an interface according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to FIG 1, an interface 2, for example a TPUART-IC, is connected to a bus system 4, in the example a two-wire bus system, ~~in particular~~ preferably an EIB. A bus ~~user~~ node 6 is connected via the interface 2, to the bus system 4 which contains the specific ~~user~~ electronics for this bus ~~user~~ node 6.

The bus ~~user~~ node 6 is preferably supplied with an external supply voltage Vext from a voltage source 8 which is independent of the

bus. The voltage source 8 is independent of the bus, for example, in the sense that the supply voltage Vext which is generated by it is independent of the bus voltage and does not load the bus system 4.

The voltage source 8 which is independent of the bus is connected to a voltage input 10 of the interface 2. The interface 2 makes available at a voltage output 12, an internal supply voltage Vcc which is generated internally from the bus voltage of the bus system 4 and is provided for supplying voltage to a bus ~~user~~ node which is not connected to a voltage source 8 which is independent of the bus. In the exemplary embodiment, this voltage output 12 is not connected to the bus ~~user~~ node 6 because the latter is supplied via the external voltage source 8. The exchange of data TxD and RxD between the bus system 4 and the bus ~~user~~ node 6 takes place via transmitting and receiving lines 14 and 16, respectively. The interface 2 and the bus ~~user~~ node 6 are connected to the same reference potential M via a ground line 18.

An output control signal R is present at a control output 20 of the interface 2 and is passed on to a voltage input 24 of the bus ~~user~~ node 6 via a control line 22. This output control signal R is a binary signal with two possible state values which releases the bus ~~user~~ node 6 to receive and transmit data.

According to FIG 2, the interface 2 preferably contains a monitoring circuit 30 with a comparator 32 with which the internal supply voltage Vcc which is derived from the bus voltage is compared with the external supply voltage Vext. The external supply voltage Vext is preferably connected to ground M via a protective resistor R and a Zener diode Z which is connected in series therewith. The positive input of the comparator 32 is connected between the Zener diode Z and the protective resistor R1.

As soon as the external supply voltage Vext exceeds the Zener voltage of the Zener diode Z, a constant external reference voltage Vref,ext corresponding to the Zener voltage is applied to the positive input of the comparator 32. This external reference voltage Vref,ext is compared with an internal reference voltage Vref,int which is derived from the internal supply voltage Vcc and made available via a voltage divider circuit R2, R3. The comparator 32 generates, at its output, a binary internal control signal S which is dependent on the sign of the difference between the external reference voltage Vref,ext and the internal supply voltage Vcc. This internal control signal S is transmitted to the gate of a MOSFET 34 whose DRAIN is connected to the control output 20.

The MOSFET 34 is in the off state if there is no control voltage (internal control signal S = low) present at the output of the comparator 32. This is the case whenever the comparator 32 supplied by the external voltage supply is not operationally capable because there is no external supply voltage Vext, or an insufficient external supply voltage Vext, or the internal reference voltage Vref,int is less than the external reference voltage Vref,ext.

In this way, the output control signal R which assumes the values zero (low) and Vext (high) in the exemplary embodiment is generated from the internal control signal S from the external supply voltage Vext. The voltage value for the high state can be set as desired between zero and Vext by means of suitable voltage line switching.

Switched in parallel with the MOSFET 34 is a further MOSFET 36 whose gate is connected to an internal module 38 which generates a control voltage for the gate of the MOSFET 36 from the internal supply voltage Vcc so

that ~~said~~ the MOSFET 36 can generate the output control signal R instead of the MOSFET 34.

Ame

In order to maintain the operational capability of the interface 2 even when there is no external voltage supply, in such a mode of operation the voltage output 12 is preferably short-circuited to the voltage input 20, as illustrated in ~~the~~ figure 2 by a bridge 40 shown by dotted and dashed lines.

VARIATIONS OF

MARKED-UP CLAIMS

What is claimed is:

Patent claims

comprising

1. (Amended) An interface [(2)] for coupling a bus [user (6)] node to [the] a bus line of a bus system [(4)], [having] an input [(10)] for an external supply voltage [(Vext)] which is made available [by] supplied by a voltage source [(8)] which is independent of the bus [,] and [having] a monitoring circuit [(30)] for comparing an internal supply voltage [(Vcc) which is] derived from the bus voltage [with] using the external supply voltage [(Vext)], and for generating an output control signal [(R)] for the bus [user (6)] node based upon a [as a function of the] result of the comparison.

2. (Amended) The interface [(2)] as claimed in claim 1, [in which] wherein the output control signal [(R)] is a binary signal whose value is determined by [the] a sign of [the] a difference between an internal reference voltage [(Vref,int)] and an external reference voltage [(Vref,ext)], respectively derived from the internal supply voltage [(Vcc)] and the external supply voltage [(Vext)].

3. (Amended) [The] A bus system [having] comprising an interface [(2)] as claimed in claim 1 [or 2], and [having] including a voltage source [(8)] [which is] independent of the bus line, for supplying at least one bus [user (6)]. node

4. (Amended) The bus system [having] comprising an interface [(2)] as claimed in claim 1 [or 2], [in which] wherein in the case of [at] a bus subscriber [(6)] which is supplied by the internal supply voltage [(Vcc)], the input [(10)] for the external supply voltage [(Vext)] is short-circuited to the voltage output [(12)] of the internal supply voltage [(Vcc)].

5. NEW same as 3, but dep on 2

6. same as 4, but dep on 2

7. same as 1, except "an input means for receiving an external...", instead of "an input for ..." external + "a monitoring means" instead of "a monitoring circuit"

8. same as 2, but dep on 7

9. same as 3, but "voltage source means" + dep on 7

10. same as 9, but dep on 8

" same as 4, but dep on 7 + "input means"

MARKED-UP ABSTRACT

GR 99 P 3387

Abstract

~~Interface for coupling a bus user to the bus line of~~ a bus system

~~According to the~~ invention, ~~the~~ An interface ~~(2)~~ for coupling a bus ~~user (6)~~ node to the bus line of a bus ~~systems (4)~~ system includes ~~contains~~ an input ~~(10)~~ for an external supply voltage ~~(Vext)~~ which is made available by a voltage source ~~(8),~~ ~~which is~~ is included, independent of the bus, ~~and~~ a monitoring circuit ~~(30)~~ for comparing an internal supply voltage ~~(Vcc)~~ which is derived from the bus voltage with the external supply voltage ~~(Vext)~~, and for generating an output control signal ~~(R)~~ for the bus ~~user (6)~~ node as a function of the result of the comparison.

~~FIG 1~~

SUBSTITUTE SPECIFICATION

INTERFACE FOR COUPLING A BUS NODE TO THE BUS LINE OF A BUS SYSTEM

[0001] This application is the national phase under 35 U.S.C. § 371 of PCT International Application No. PCT/DE00/01712 which has an International filing date of May 26, 2000, which designated the United States of America, the entire contents of which are hereby incorporated by reference.

Field of the Invention

[0002] The invention generally relates to an interface. More specifically, it relates to an interface for coupling a bus node to the bus line of a bus system. Preferably, it relates to the bus system EIB of the European Installation Bus Association EIBA.

Background of the Invention

[0003] The bus system of the EIB is a two-wire bus system in which the voltage supply of the bus nodes, which are respectively connected to the bus system via an interface, and the data transmission between the latter are combined on one pair of lines. In this type of bus system, the power drain per bus node is limited to 10 mA, for example. However, such a limited power drain is not sufficient for all the bus nodes in all applications. Thus, it may be necessary to supply an external voltage to bus nodes with a higher power requirement. Such an additional external supply voltage which is independent of the bus can also be advantageous for relieving the loading on the voltage supply of the EIB.

[0004] In such a case, the situation arises in which, although the interface for example a TPUART-IC, is supplied from the EIB cell, the bus node which is connected to the bus system via this interface is fed from an external voltage supply which is independent of the latter.

[0005] An interface which is used with the EIB generates a control signal (reset signal) for the bus node with which, inter alia, the exchange of data is enabled only if the supply voltage of the bus node has reached a predefined value, and the bus node has also been given sufficient time for a correct run-up. When there is no bus voltage, or insufficient bus voltage, the interface outputs a value for a binary control signal, for example low (= reset active), which ensures that an exchange of data cannot take place. The control signal is not set to another value, for example high (= reset inactive) and an exchange of data made possible until both the supply voltage of the interface and the bus voltage which is transmitted from the interface to the bus node has reached a predefined value.

[0006] In the case of a bus node which is supplied via an external power supply unit, an operating situation may then occur in which, on the one hand, the bus voltage is not yet present at a sufficient level. On the other hand, the external voltage supply for the bus node is already present so that the bus node is active, but the interface itself has not yet been supplied with a sufficient supply voltage necessary for its operation. In this case, an attempt by the bus node to transmit would lead to a fault message.

[0007] JP 01 193 953 A discloses a system for detecting abnormality of bus, and DE 196 39 635 C discloses a CMOS bus driver circuit.

SUMMARY OF THE INVENTION

[0008] The invention is based on an object of disclosing an interface for coupling a bus node to the bus line of a bus system; preferably one with which the faulty operating state specified above is avoided.

[0009] The object is achieved, for example, by the invention with an interface having the features of patent claim 1. The interface preferably contains an input for an external supply voltage which is made available by a voltage source which is independent of the bus, and a

monitoring circuit for comparing an internal supply voltage which is derived from the bus voltage with the external supply voltage, and for generating an output control signal for the bus node as a function of the result of the comparison. This measure ensures that the bus node is enabled only if the interface is also in a satisfactory operating state.

[00010] In one preferred embodiment of the invention, the output control signal is a binary signal whose value is determined by the sign of the difference between an internal reference voltage and an external reference voltage, respectively derived from the internal supply voltage and the external supply voltage. Such an interface is preferably provided in particular for use in a bus system which contains at least one bus node which is supplied with an external supply voltage from a voltage source which is independent of the bus.

[00011] The interface preferably cannot be used for coupling a bus node supplied by the bus voltage. For this purpose, in one advantageous configuration of the invention, all that is necessary is to short-circuit the input of the external supply voltage to an output for the internal supply voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[00012] In order to explain the invention further, reference is made to the exemplary embodiment in the drawing, in which:

FIG 1 shows an interface according to the invention with a bus node connected thereto, in a block circuit diagram,

FIG 2 shows an advantageous configuration of a monitoring circuit for an interface according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[00013] According to FIG 1, an interface 2, for example a TPUART-IC, is connected to a bus system 4, in the example a two-wire bus system, preferably an EIB. A bus node 6 is

connected via the interface 2, to the bus system 4 which contains the specific electronics for this bus node 6.

[00014] The bus node 6 is preferably supplied with an external supply voltage Vext from a voltage source 8 which is independent of the bus, for example. The voltage source 8 is independent of the bus in the sense that the supply voltage Vext which is generated by it is independent of the bus voltage and does not load the bus system 4.

[00015] The voltage source 8 which is independent of the bus is connected to a voltage input 10 of the interface 2. The interface 2 makes available at a voltage output 12, an internal supply voltage Vcc which is generated internally from the bus voltage of the bus system 4 and is provided for supplying voltage to a bus node which is not connected to a voltage source 8 which is independent of the bus. In the exemplary embodiment, this voltage output 12 is not connected to the bus node 6 because the latter is supplied via the external voltage source 8. The exchange of data TxD and RxD between the bus system 4 and the bus node 6 takes place via transmitting and receiving lines 14 and 16, respectively. The interface 2 and the bus node 6 are connected to the same reference potential M via a ground line 18.

[00016] An output control signal R is present at a control output 20 of the interface 2 and is passed on to a voltage input 24 of the bus node 6 via a control line 22. This output control signal R is a binary signal with two possible state values which releases the bus node 6 to receive and transmit data.

[00017] According to FIG 2, the interface 2 preferably contains a monitoring circuit 30 with a comparator 32 with which the internal supply voltage Vcc which is derived from the bus voltage is compared with the external supply voltage Vext. The external supply voltage Vext is connected to ground M via a protective resistor R and a Zener diode Z which is preferably connected in series therewith. The positive input of the comparator 32 is connected between

the Zener diode Z and the protective resistor R1. As soon as the external supply voltage Vext exceeds the Zener voltage of the Zener diode Z, a constant external reference voltage Vref,ext corresponding to the Zener voltage is applied to the positive input of the comparator 32. This external reference voltage Vref,ext is compared with an internal reference voltage Vref,int which is derived from the internal supply voltage Vcc and made available via a voltage divider circuit R2, R3. The comparator 32 generates, at its output, a binary internal control signal S which is dependent on the sign of the difference between the external reference voltage Vref,ext and the internal supply voltage Vcc. This internal control signal S is transmitted to the gate of a MOSFET 34 whose DRAIN is connected to the control output 20.

[00018] The MOSFET 34 is in the off state if there is no control voltage (internal control signal S = low) present at the output of the comparator 32. This is the case whenever the comparator 32 supplied by the external voltage supply is not operationally capable because there is no external supply voltage Vext, or an insufficient external supply voltage Vext, or the internal reference voltage Vref,int is less than the external reference voltage Vref,ext.

[00019] In this way, the output control signal R which assumes the values zero (low) and Vext (high) in the exemplary embodiment is generated from the internal control signal S from the external supply voltage Vext. The voltage value for the high state can be set as desired between zero and Vext by means of suitable voltage line switching.

[00020] Switched in parallel with the MOSFET 34 is a further MOSFET 36 whose gate is connected to an internal module 38 which generates a control voltage for the gate of the MOSFET 36 from the internal supply voltage Vcc so that the MOSFET 36 can generate the output control signal R instead of the MOSFET 34.

[00021] In order to maintain the operational capability of the interface 2 even when there is no external voltage supply, in such a mode of operation the voltage output 12 is preferably

short-circuited to the voltage input 20, as illustrated in figure 2 by a bridge 40 shown by dotted and dashed lines.

[00022] The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
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(81) Bestimmungsstaaten *(national)*: AU, CN, US.

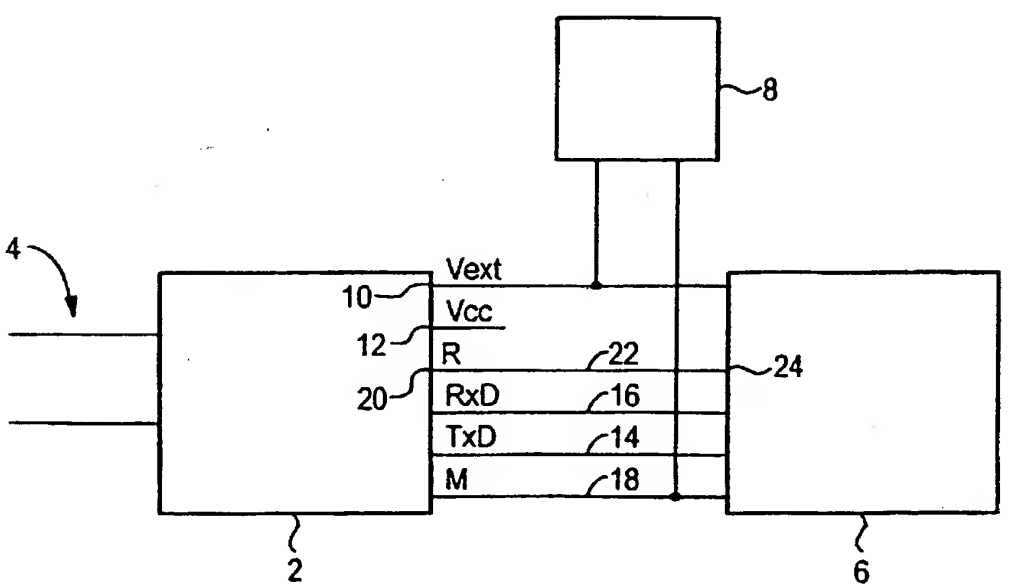
(84) Bestimmungsstaaten *(regional)*: europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Veröffentlicht:
— *Mit internationalem Recherchenbericht.*

[Fortsetzung auf der nächsten Seite]

(54) Title: INTERFACE FOR COUPLING A BUS NODE TO THE BUS LINE OF A BUS SYSTEM

(54) Bezeichnung: INTERFACE ZUM ANKOPPELN EINES BUSTEILNEHMERS AN DIE BUSLEITUNG EINES BUSSYSTEMS



(57) Abstract: The invention relates to an interface (2) for coupling a bus node (6) to the bus line of a bus system (4). According to the invention, the inventive interface comprises an input (10) for an external supply voltage (Vext) which is provided by a bus-independent voltage source (8), and comprises a monitoring circuit (30). Said monitoring circuit is provided for comparing an internal supply voltage (Vcc) derived from the bus voltage with the external supply voltage (Vext) and for generating an output control signal (R) for the bus node (6) based on the result of the comparison.

[Fortsetzung auf der nächsten Seite]

WO 00/75794 A1

Description

Interface for coupling a bus user to the bus line of a bus system

The invention relates to an interface for coupling a bus user to the bus line of a bus system, in particular to the bus system EIB of the European Installation Bus Association EIBA.

The bus system EIB is a two-wire bus system in which the voltage supply of the bus users which are respectively connected to the bus system via an interface and the data transmission between the latter are combined on one pair of lines. In this type of bus system, the power drain per bus user is limited to 10 mA, for example. However, such a limited power drain is not sufficient for all the bus users in all applications so that it may be necessary to supply an external voltage to bus users with a higher power requirement. Such an additional external supply voltage which is independent of the bus can also be advantageous for relieving the loading on the voltage supply of the EIB.

In such a case, the situation arises in which although the interface, for example a TPUART-IC, is supplied from the EIB cell, the bus user which is connected to the bus system via this interface is fed from an external voltage supply which is independent of the latter.

An interface which is used with the EIB generates a control signal (reset signal) for the bus user with which, inter alia, the exchange of data is enabled only if the supply voltage of the bus user has reached a predefined value, and the bus user has also been given sufficient time for a correct run-up. When

there is no bus voltage, or insufficient bus voltage, the interface outputs a value

for a binary control signal, for example low (= reset active), which ensures that an exchange of data cannot take place. The control signal is not set to another value, for example high (= reset inactive) and an exchange of data made possible until both the supply voltage of the interface and the bus voltage which is transmitted from the interface to the bus user has reached a predefined value.

In the case of a bus user which is supplied via an external power supply unit, an operating situation may then occur in which, on the one hand, the bus voltage is not yet present at a sufficient level, but, on the other hand, the external voltage supply for the bus user is already present so that the bus user is active, but the interface itself has not yet been supplied with a sufficient supply voltage necessary for its operation. In this case, an attempt by the bus user to transmit would lead to a fault message.

JP 01 193 953 A discloses a system for detecting abnormality of bus, and DE 196 39 635 C discloses a CMOS bus driver circuit.

The invention is then based on the object of disclosing an interface for coupling a bus user to the bus line of a bus system with which the faulty operating state specified above is avoided.

The aforesaid object is achieved according to the invention with an interface having the features of patent claim 1. The interface according to the invention contains an input for an external supply voltage which is made available by a voltage source which is independent of the bus, and a monitoring circuit for comparing an internal supply voltage which

is derived from the bus voltage with the external supply voltage, and for generating an output control signal for the bus user as a function of the result of the comparison. This measure ensures that the bus user is enabled only if the interface is also in a satisfactory operating state.

In one preferred embodiment of the invention, the output control signal is a binary signal whose value is determined by the sign of the difference between an internal reference voltage and an external reference voltage, respectively derived from the internal supply voltage and the external supply voltage. Such an interface according to the invention is provided in particular for use in a bus system which contains at least one bus user which is supplied with an external supply voltage from a voltage source which is independent of the bus.

The interface according to the invention cannot be used for coupling a bus user supplied by the bus voltage. For this purpose, in one advantageous configuration of the invention all that is necessary is to short-circuit the input of the external supply voltage to an output for the internal supply voltage.

In order to explain the invention further, reference is made to the exemplary embodiment in the drawing, in which:

FIG 1 shows an interface according to the invention with a bus user connected thereto, in a block circuit diagram,

FIG 2 shows an advantageous configuration of a monitoring circuit for an interface according to the invention.

According to FIG 1, an interface 2, for example a TPUART-IC, is connected to a bus system 4, in the example a two-wire bus system, in particular an EIB. A bus user 6 is connected via the interface 2 to the bus system 4 which contains the specific user electronics for this bus user 6.

The bus user 6 is supplied with an external supply voltage Vext from a voltage source 8 which is independent of the

bus. The voltage source 8 is independent of the bus in the sense that the supply voltage Vext which is generated by it is independent of the bus voltage and does not load the bus system 4.

The voltage source 8 which is independent of the bus is connected to a voltage input 10 of the interface 2. The interface 2 makes available at a voltage output 12 an internal supply voltage Vcc which is generated internally from the bus voltage of the bus system 4 and is provided for supplying voltage to a bus user which is not connected to a voltage source 8 which is independent of the bus. In the exemplary embodiment, this voltage output 12 is not connected to the bus user 6 because the latter is supplied via the external voltage source 8. The exchange of data TxD and RxD between the bus system 4 and the bus user 6 takes place via transmitting and receiving lines 14 and 16, respectively. The interface 2 and the bus user 6 are connected to the same reference potential M via a ground line 18.

An output control signal R is present at a control output 20 of the interface 2 and is passed on to a voltage input 24 of the bus user 6 via a control line 22. This output control signal R is a binary signal with two possible state values which releases the bus user 6 to receive and transmit data.

According to FIG 2, the interface 2 contains a monitoring circuit with a comparator 32 with which the internal supply voltage Vcc which is derived from the bus voltage is compared with the external supply voltage Vext. The external supply voltage Vext is connected to ground M via a protective resistor R and a Zener diode Z which is connected in series therewith. The positive input of the comparator 32 is connected between the Zener diode Z and the protective resistor R1.

As soon as the external supply voltage Vext exceeds the Zener voltage of the Zener diode Z, a constant external reference voltage Vref,ext corresponding to the Zener voltage is applied to the positive input of the comparator 32. This external reference voltage Vref,ext is compared with an internal reference voltage Vref,int which is derived from the internal supply voltage Vcc and made available via a voltage divider circuit R2, R3. The comparator 32 generates, at its output, a binary internal control signal S which is dependent on the sign of the difference between the external reference voltage Vref,ext and the internal supply voltage Vcc. This internal control signal S is transmitted to the gate of a MOSFET 34 whose DRAIN is connected to the control output 20.

The MOSFET 34 is in the off state if there is no control voltage (internal control signal S = low) present at the output of the comparator 32. This is the case whenever the comparator 32 supplied by the external voltage supply is not operationally capable because there is no external supply voltage Vext, or an insufficient external supply voltage Vext, or the internal reference voltage Vref,int is less than the external reference voltage Vref,ext.

In this way, the output control signal R which assumes the values zero (low) and Vext (high) in the exemplary embodiment is generated from the internal control signal S from the external supply voltage Vext. The voltage value for the high state can be set as desired between zero and Vext by means of suitable voltage line switching.

Switched in parallel with the MOSFET 34 is a further MOSFET 36 whose gate is connected to an internal module 38 which generates a control voltage for the gate of the MOSFET 36 from the internal supply voltage Vcc so

that said MOSFET 36 can generate the output control signal R instead of the MOSFET 34.

Ame

In order to maintain the operational capability of the interface 2 even when there is no external voltage supply, in such a mode of operation the voltage output 12 is short-circuited to the voltage input 20, as illustrated in the figure by a bridge 40 shown by dotted and dashed lines.

Patent claims

1. An interface (2) for coupling a bus user (6) to the bus line of a bus system (4), having an input (10) for an external supply voltage (Vext) which is made available by a voltage source (8) which is independent of the bus, and having a monitoring circuit (30) for comparing an internal supply voltage (Vcc) which is derived from the bus voltage with the external supply voltage (Vext), and for generating an output control signal (R) for the bus user (6) as a function of the result of the comparison.

2. The interface (2) as claimed in claim 1, in which the output control signal (R) is a binary signal whose value is determined by the sign of the difference between an internal reference voltage (Vref,int) and an external reference voltage (Vref,ext), respectively derived from the internal supply voltage (Vcc) and the external supply voltage (Vext).

3. The bus system having an interface (2) as claimed in claim 1 or 2, and having a voltage source (8) which is independent of the bus, for supplying at least one bus user (6).

4. The bus system having an interface (2) as claimed in claim 1 or 2, in which in the case of at a bus subscriber (6) which is supplied by the internal supply voltage (Vcc), the input (10) for the external supply voltage (Vext) is short-circuited to the voltage output (12) of the internal supply voltage (Vcc).

GR 99 P 3387

Abstract

Interface for coupling a bus user to the bus line of a bus system

According to the invention, the interface (2) for coupling a bus user (6) to the bus line of a bus systems (4) contains an input (10) for an external supply voltage (Vext) which is made available by a voltage source (8) which is independent of the bus, and a monitoring circuit (30) for comparing an internal supply voltage (Vcc) which is derived from the bus voltage with the external supply voltage (Vext), and for generating an output control signal (R) for the bus user (6) as a function of the result of the comparison.

FIG 1

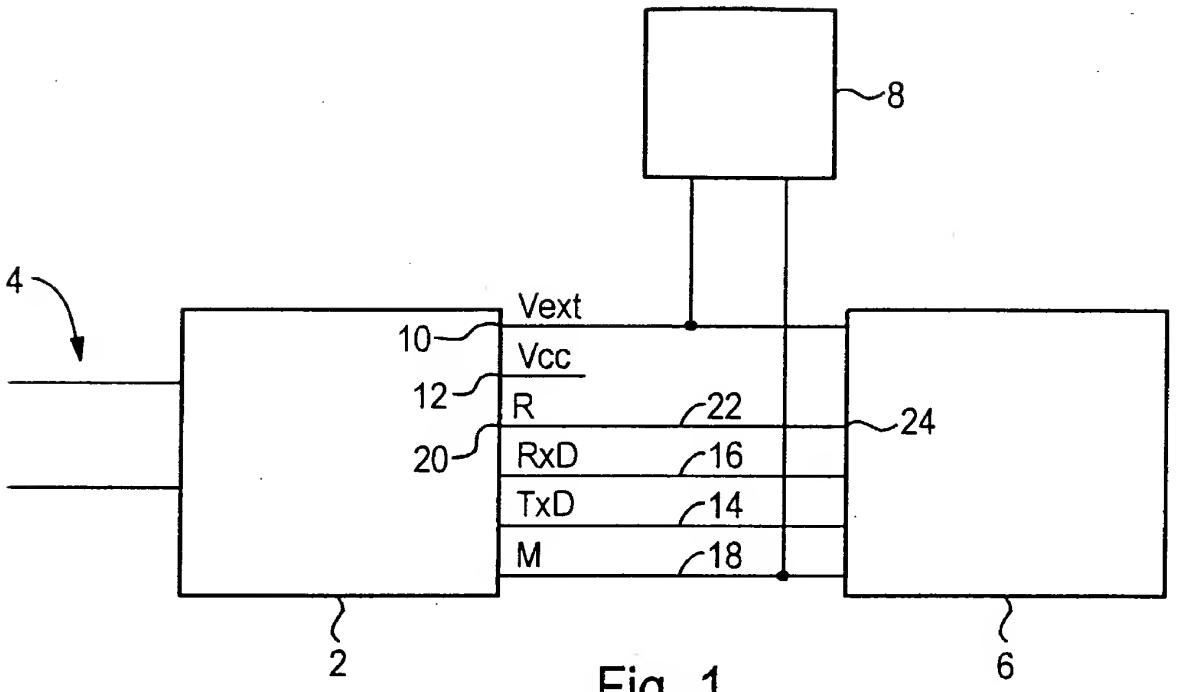


Fig. 1

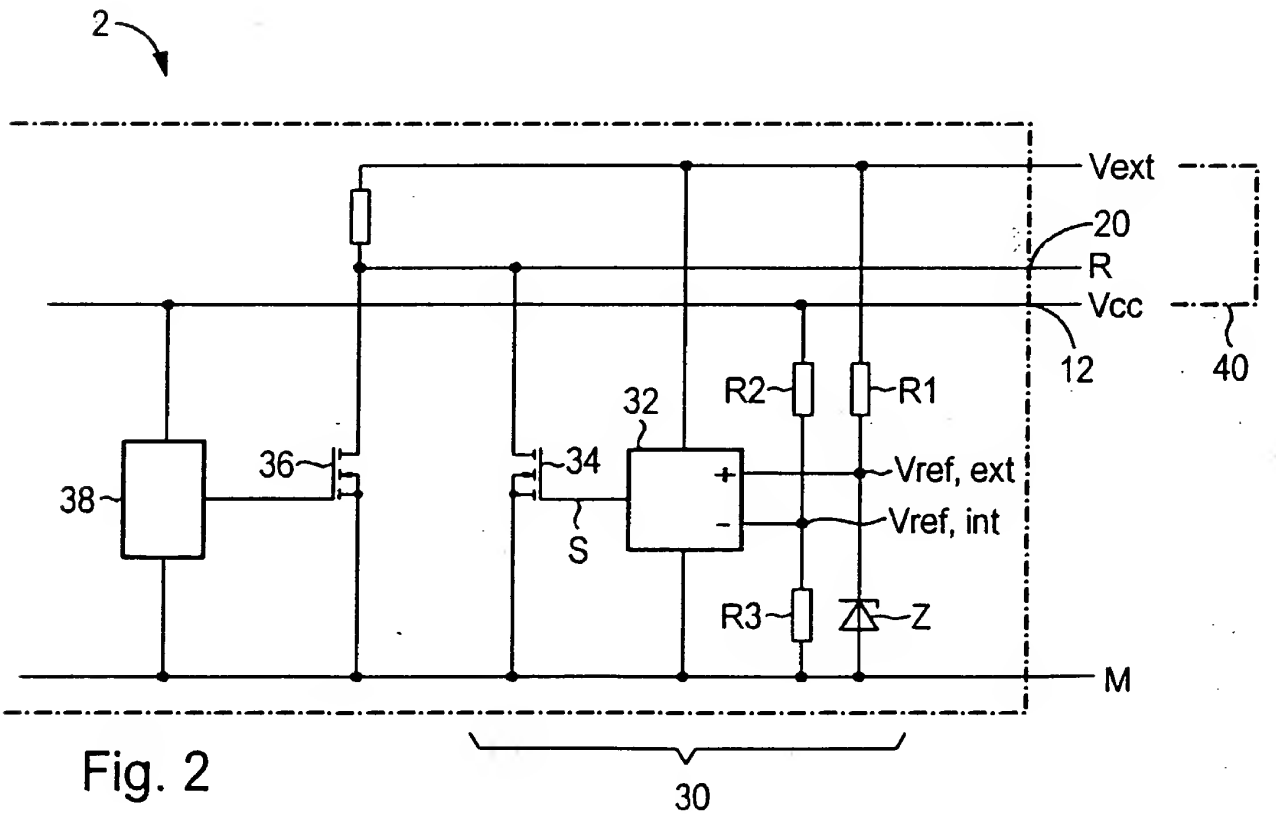


Fig. 2

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Interface zum Ankoppeln eines Busteilnehmers an die Busleitung eines Bussystems

Interface for coupling a bus node to the bus line of a bus system

deren Beschreibung

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 26.05.2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE00/01712
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

the specification of which

(check one)
☐ is attached hereto.
☒ was filed on 26.05.2000 as
PCT international application
PCT Application No. PCT/DE00/01712
and was amended on _____
(if applicable)

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

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German Language Declaration

Prior foreign appplications
Priorität beansprucht

			Priority Claimed	
19926095.8	DE	08.06.1999	☒	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

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PCT/DE00/01712	26.05.2000		pending
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(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

And I hereby appoint

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Unterschrift des Erfinders / Datum	Inventor's signature / Date: Norbert Fichtner 23.11.01
Wohnsitz: Schierling, DEUTSCHLAND	Residence: Schierling, GERMANY D EX
Staatsangehörigkeit: DEUTSCH	Citizenship: GERMAN
Postanschrift: Kaiser-Otto-Ring 30 84069 Schierling DEUTSCHLAND	Post Office Addess: Kaiser-Otto-Ring 30 84069 Schierling GERMANY
Voller Name des zweiten Miterfinders (falls zutreffend): DIETER MUNZ	Full name of second joint inventor, if any: DIETER MUNZ
Unterschrift des Erfinders / Datum	Second Inventor's signature / Date
Wohnsitz: HÖCHSTADT, DEUTSCHLAND	Residence: HÖCHSTADT, GERMANY D EX
Staatsangehörigkeit: DEUTSCH	Citizenship: GERMAN
Postanschrift: TILMANN-RIEMENSCHNEIDER-STR. 19 91315 HÖCHSTADT DEUTSCHLAND	Post Office Address: TILMANN-RIEMENSCHNEIDER-STR. 19 91315 HÖCHSTADT GERMANY

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(Supply similar information and signature for third and subsequent joint inventors).

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Erklärung Für Patentanmeldungen Mit Vollmacht

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			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE00/01712	26.05.2000		pending
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D, M, Y) (Anmeldedatum T, M, J)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

And I hereby appoint

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